CLAIM AMENDMENTS

1.-24. (Cancelled)

25. (Previously Presented) A method comprising:

establishing windows of time for a first bus agent to request access to a bus;

for times outside of the windows, denying all requests from the first bus agent to access the bus;

monitoring accesses to the bus during the windows; and

selectively regulating durations of the windows in response to the monitoring.

26. (Previously Presented) The method of claim 25, wherein the first bus agent comprises:

a system controller.

27. (Currently Amended) The method of claim 25, further comprising:

for times outside of the windows, selectively granting requests from a processor ~~wherein the second bus agent comprises:~~

~~a processor~~.

28. (Previously Presented) The method of claim 25, wherein the act of monitoring comprises:

determining a number of clock cycles in which first bus agent accesses the bus during the window.

29. (Previously Presented) The method of claim 25, wherein the act of regulating comprises:

decreasing the duration of one of the windows if the amount of use by the first bus agent approximately increases above a threshold.

30. (Currently Amended) The method of claim 25, wherein the act of monitoring comprises:

counting clock cycles when the first bus agent requests ownership of the bus.

31. (Previously Presented) The method of claim 25, wherein the bus comprises:

a local bus.

32. (Cancelled)

33. (Previously Presented) A bridge usable with a first bus agent that has higher priority for accesses to a bus than a second bus agent, the bridge comprising:

a circuit adapted to:

permit the first bus agent to access the bus during windows of time and prevent the first bus agent from accessing the bus outside of the windows to permit the second bus agent to access the bus,

monitor use of the bus by the first bus agent during the windows, and

selectively regulate the durations of the windows in response to the monitored use.

34. (Previously Presented) The bridge of claim 33, wherein the first bus agent comprises a system controller and the second bus agent comprises a processor.

35. (Previously Presented) The bridge of claim 33, wherein the circuit comprises:

a timer adapted to determine a number of clock cycles in which the first bus agent accesses the bus during one of the windows.

36. (Previously Presented) The bridge of claim 33, wherein the circuit is adapted to regulate the durations by decreasing the duration of one of the windows if the amount of use of the bus by the first bus agent approximately increases above a threshold.

37. (Previously Presented) The bridge of claim 33, wherein the circuit comprises:

a timer adapted to not count clock cycles when the second bus agent accesses the bus and count clock cycles when the first bus agent accesses the bus.